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JC928 U.S. PTO 09/62/00

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PTO/SB/05 (4/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	D5116-00002
First Inventor or Application Identifier	Sharad Saxena et al.
Title	EFFICIENT METHOD FOR MODELING AND SIMULATION ...
Express Mail Label	EL379383687US

JC922 U.S. PTO 09/675427 09/29/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] *Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original, and a duplicate for fee processing)

2. [X] Specification [*Total Pages* 22]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 3]

4. Oath or Declaration [*Total Pages* 5]
a. [X] Newly executed (original or copy)
b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies.

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [X] *Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: Certification Under 37 C.F.R. 1.10 . . . . .
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16. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____
Prior application information: Examiner _____ *Group / Art Unit:* _____
For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The corporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

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Name (Print/Type)	William H. Murray	*Registration No. (Attorney/Agent)*	27,218
Signature		*Date*	September 29, 2000

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Express Mail Label No. EL379383687US

Attorney Docket No. D5116-00002

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of: Sharad Saxena et al.

Serial No.: To Be Assigned

Group Art Unit: To Be Assigned

Filed: September 29, 2000

Examiner: To Be Assigned

For: EFFICIENT METHOD FOR MODELING AND SIMULATION OF THE IMPACT OF LOCAL AND GLOBAL VARIATION ON INTERGRATED CIRCUITS

Certification Under 37 CFR 1.10

I hereby certify that this document (along with the enclosed Utility Patent Application Transmittal and any documents referred to therein) is being deposited with the United States Postal Service on the date shown below with sufficient postage as "Express Mail Post Office to Addressee" Mailing Label Number EL379383687US on September 29, 2000 to the following:

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FEE TRANSMITTAL for FY 2000

Patent fees are subject to annual revision.
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.
See 37 C.F.R. §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($)**$424.00**

Complete if Known	
Application Number	**NOT KNOWN**
Filing Date	**September 29, 2000**
First Named Inventor	**Sharad Saxena et al.**
Examiner Name	**NOT KNOWN**
Group / Art Unit	**NOT KNOWN**
Attorney Docket No.	**D5116-00002**

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: **04-1679**

Deposit Account Name: **Duane, Morris & Heckscher LLP**

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2. ☒ **Payment Enclosed:**
☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	345.00
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 345.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims 10	-20** = 0	X	0	=	0
Independent Claims 4	- 3** = 1	X	39	=	39.00
Multiple Dependent			0	=	39.00

***or number previously paid, if greater; For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 39.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension for reply within second month	
117	870	217	435	Extension for reply within third month	
118	1,360	218	680	Extension for reply within fourth month	
128	1,850	228	925	Extension for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	760	246	380	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	760	249	380	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify)					
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40.00

SUBMITTED BY

Complete *(if applicable)*

Name (Print/Type)	**William H. Murray**	*Registration No. (Attorney/Agent)*	**27,218**	*Telephone*	**(215) 979-1264**
Signature				*Date*	**September 29, 2000**

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APPLICANT OR PATENTEE: Sharad Saxena et al.

ATTORNEY DOCKET NO.: D5116-00002

SERIAL OR PATENT NO.:

DATE FILED OR ISSUED: Herewith

FOR: EFFICIENT METHOD FOR MODELING AND SIMULATION OF THE IMPACT OF LOCAL AND GLOBAL VARIATION ON INTERGRATED CIRCUITS

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) and 1.27(c)) - SMALL BUSINESS CONCERN

I hereby declare that I am:

[ ] the owner of the small business concern identified below:

[X] an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: PDF Solutions, Inc.

ADDRESS OF CONCERN: 333 West San Carlos, Suite 700
San Jose, California 95110

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either directly or indirectly, one concern controls or has the power to control the other, or a third-party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled EFFICIENT METHOD FOR MODELING AND SIMULATION OF THE IMPACT OF LOCAL AND GLOBAL VARIATION ON INTERGRATED CIRCUITS by inventors Sharad Saxena, Carlo Guardiani, Philip D. Schumaker, Patrick D. McNamara, and Dale Coder filed herewith.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27).

NAME: PDF Solutions, Inc.

ADDRESS: 333 West San Carlos Street, Suite 700
San Jose, California 95110

[ ] Individual [X] Small Business Concern [ ] Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small business entity is no longer appropriate. (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statement and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING:

TITLE OR PERSON OTHER THAN OWNER:

ADDRESS OF PERSON SIGNING:

SIGNATURE _____ **Date:** 9/18/02

PH3\618724.1

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application Serial No. 60/166,242 filed on November 18, 1999, the contents of which is incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

The present invention pertains to fabrication of integrated circuits and more particularly to methods and systems for analyzing the performance and manufacturability of integrated circuits.

Miniaturization and scaling of integrated circuits have resulted in two conflicting trends. On one hand, margins available in high-performance designs are shrinking, increasing the likelihood that inevitable variations during manufacturing will cause performance violations. On the other hand, both the amount of variation as a fraction of the feature sizes, and the sensitivity of the characteristics of transistors and interconnects to manufacturing variations is increasing. This makes it essential to model and simulate accurately and efficiently the impact of manufacturing variations on the performance of integrated circuits.

Manufacturing variations include intra-die variations, hereinafter referred to as "local mismatch", and inter-die variations, hereinafter referred to as "global variations". Such intra-die and global variations are random and systematic variations in the material composition, or in the processing steps that are used to fabricate the integrated circuits. Local mismatch, or intra-die variations, are differences in the electrical properties of circuit elements that affect components of the circuits that are fabricated on the same die. For example, two identically drawn transistors fabricated

next to each other in any particular chip will still present different threshold voltage values. Global variations, or inter-die variations, affect integrated circuit devices by causing random differences in the electrical properties of circuit elements, such as transistors, resistors, capacitors, memory cells, wires, etc., that are fabricated on different chips from the same wafer, on different wafers, or on different batches of wafers. As circuits are designed assuming i) a given nominal value of the electrical properties of its elements and ii) that identically drawn elements behave exactly in the same way, both global variations and local mismatch affect the actual circuit performance and are essential to determine the yield of the product.

Local mismatch has not been adequately modeled in the past. Accurate matching of the electrical properties of active and passive elements is fundamental for functional and parametric performances of analog and mixed-signal integrated performance (IP) blocks, such as operational amplifiers (OPAMPs), digital to analog (D/A) and analog to digital (A/D) converters, phase locked loops (PLLs), etc. Achieving target functional and parametric yield of analog and mixed-signal components frequently represents a major bottleneck for the global time-to-volume performance of complex very large scale integrated (VLSI) systems.

Previous work in modeling and analysis of matching properties of electronic devices, such as that described in the paper entitled *"Matching Properties of MOS Transistors ", Pelgrom M., Dunjnmayer, A., and Welbers A., IEEE Journal of Solid State Circuits, Vol SC-24, pp 1433-1440, October 1989*, which paper is incorporated by reference in this detailed description as if fully set forth herein, aims at deriving a suitable model of intra-die metal oxide semiconductor

field effect transistor (MOSFET) variance as a function of device size, layout distance and orientation. Although these models have become popular, their direct application in the context of electrical circuit simulation is difficult for two main reasons.

First, they model the matching properties of MOSFET "*macro*" characteristics, such as threshold voltage (V_{Th}) or saturation current (I_{DSAT}) that are only indirectly related to the actual "*low-level*" parameters of most widely used compact SPICE (System Program for Integrated Circuits Emphasis) simulation models, such as BSIM3v3 (*"MOSFET Modeling and BSIM User Guide, Cheng, Y. and Hu, C., Kluwer Academic Publishers, Boston, 1999,* incorporated by reference as if fully set forth herein) or MOS9 (*"Compact Modeling for Analogue Circuit Simulation", Velghe, R., et al., IEDM Tech. Digest, pp. 485-488, 1993,* incorporated by reference as if fully set forth herein). Therefore, a non-trivial inverse modeling process must be applied to extract the proper covariance structure of low-level SPICE model parameters corresponding to the available matching characterization data for these macro parameters.

Second, applying a device level mismatch model to the statistical simulation of electronic circuits requires the assumption that every matched device is described by a different set of low-level device parameters, each associated with a corresponding random variable (RV) (*"Statistical Modeling of Device Mismatch for Analog Integrated Circuits", Michael, C. and Ismail, M., IEEE Journal of Solid-State Circuits, Vol 27, No 2, February 1992; "Applying a Submicron Mismatch Model to Practical IC Design", Guardiani, C. et al., IEEE CICC Conference, May 1994; "Hierarchical Statistical Circuit Characterization of Mixed-Signal Circuits using Behavioral*

Modeling", Felt et al., IEEE-ACM International Conference on Computer Aided Design, San Jose, CA, November 1996, all of which are incorporated by reference as if fully set forth herein). The variance of the relevant circuit performance parameters can then be estimated via Monte-Carlo analysis. This process requires the generation of a sequence of correlated vectors of random numbers, and the evaluation of the circuit performance corresponding to each random vector instance either by directly using SPICE or via RSM macro-modeling. The dimensionality of the corresponding RV space can be very large when the simultaneous variation of all matched n-tuples of devices is considered.

The problem associated with the large dimensionality of the mismatch simulation task has not yet been properly addressed. The σ-space approach of Michael and Ismail (cited above), which can be proven to be equivalent to the Choleski factorization technique used by Felt et al. (cited above), requires $\sum_{i=1}^{nd} (N(m_j) - 1) X N(p_j)$ different RVs, where, $N(m_j)$ is the number of matched devices of type j, $N(p_j)$ is the number of independent process factors used in the model of the j th device type, and nd is the number of different devices in the circuit.

The empirical approach of Guardiani et al. (cited above), has an even greater complexity, and can be only applied to very simple circuits. Conti (*"Parametric Yield Formulation of MOS ICs affected by mismatch effect", Conti, M., IEEE Transactions on Computer Aided Design, vol 18, pp. 582 -596, May 1999*, incorporated by reference as if fully set forth herein) proposed a method based on the experimental characterization of a parametrized auto-correlation function for the relevant process parameters described as spatial stochastic processes. The autocorrelation

function is then used to derive a symbolic formula for the system covariance matrix as a function of the layout parameters. Therefore, the complexity of this methodology is also proportional to the same number of variables as the σ-space approach, however this technique is compatible with the statistical simulation methodology described herein, and can be used to replace the approach of deriving the component correlation matrix using a mismatch model.

SUMMARY OF THE INVENTION

A method of modeling and simulating the impact of global and local variation on the performance of integrated circuits includes the steps of estimating a representation of component mismatch from device performance measurements in a form suitable for circuit simulation; reducing the complexity of statistical simulation by performing a first level principal component or principal factor decomposition of global variation, including screening; further reducing the complexity of statistical simulation by performing a second level principal decomposition including screening for each factor retained in the step of reducing the complexity; and performing statistical simulation with the joint representation of global and local variation obtained in the step of further reducing the complexity.

A method of modeling and simulating the impact of global and local variation on the performance of integrated circuits includes the following steps. First, convert, if necessary, the device mismatch model at the device performance level into a model suitable for circuit simulation, that is, at the SPICE parameter level. Second, if the global variation is provided, perform a first level principal-component or principal-factor decomposition and screening to

represent the global variation. If no global variation is provided, perform this decomposition for the local variation alone. Third, perform a second level principal-component or principal-factor decomposition and screening for each independent factor identified in the second step to represent the local variation and reduce its dimensionality. If no global variation is explained in the initial model before local variation is applied, this step does not apply. Fourth, perform statistical circuit simulation and analysis with the combined set of independent factors that result from the second and/or third steps to estimate the impact of global and local variation jointly and/or separately on the circuit of interest.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic of a low-voltage opamp used for illustrating the method of the present invention.

Figure 2 is a histogram showing the impact of mismatch on the input offset voltage of the opamp shown in Figure 1.

Figure 3 is a block diagram of a digital to analog converter used for illustrating the method of the present invention on circuits involving matching of more that two components at a time.

Figure 4 is a graph showing the efficiency of principal component analysis followed by screening in reducing the complexity of statistical simulation including global and local effects.

DETAILED DESCRIPTION OF THE INVENTION

In accordance with the present invention, an efficient representation of both inter-die and intra-die variation is constructed to analyze the joint impact of these sources of process variation on a design. The impact of manufacturing variations on a component is typically represented by estimating the distribution of SPICE model parameters for that component. A statistical SPICE model that represents both inter-die and intra-die variations has to account for two types of correlation; that is, correlation between model parameters and correlation between matched components. The correlation between model parameters arises because most commonly used SPICE models utilize non-independent parameters. The correlation between different components on the same die arises because of intra-die process variation.

Both the inter-die and intra-die correlation can be represented in a single correlation matrix. Given n matched components $(C_1,...,C_n)$ and a SPICE model for each component with m parameters $(P_1,...P_m)$, a straight-forward implementation would construct a $nm \times nm$ correlation matrix:

$$\begin{bmatrix} 1 & \rho_{11,12} & \cdots & \rho_{11,nm} \\ \rho_{12,11} & 1 & \cdots & \rho_{12,nm} \\ \cdots & \cdots & \cdots & \cdots \\ \rho_{nm,11} & \cdots & \rho_{nm,n(m-1)} & 1 \end{bmatrix} \quad (1)$$

where the rows and columns are T_ip_j, representing parameter j for transistor i. The element $\rho_{ij,kl}$

represents the correlation between $T_i p_j$ and $T_k p_l$.

This representation is computationally very expensive since the matrix grows as $0(nm \times nm)$. Two simplifications are realized by using principal component (PC) decomposition. The first simplification is the use of PCS to represent the correlation between the model parameters and the second simplification is the use of PCS to represent the correlation between the matched devices.

Inter-die Principal Component Decomposition

Principal component representation expresses a set of correlated random variables in terms of a set of independent random variables. This is obtained by applying a congruence transformation of the form: $\Gamma\Sigma\Gamma^T = \Lambda$ to the covariance (or correlation) matrix Σ, such that Γ is an orthogonal matrix and Λ is diagonal matrix, its elements λ_{ii} are the eigenvalues of the covariance matrix. An important property of principal component decomposition is that:

$$\sigma_q^2 = \left(\sum_{i=1}^{q} \lambda_{ii}\right) / \left(\sum_{i=1}^{n} \lambda_{ii}\right) \qquad (2)$$

represents the fraction of the variance explained by the first $_q$ PCs. By replacing the model parameters $(p_{1,\ldots}p_n)$ by PCS $(f_1,\ldots,f_k)$ in the Eq. (1) one gets a $nk \times nk$ size matrix, where typically $k \ll m$. The reduction in the matrix size stems from the application of a suitable threshold filtering algorithm based on Eq. (2). However, further simplifications are possible because using PCS instead of model parameters makes the correlation matrix very sparse. Because the PCS are

independent, the correlation between different factors for the same component is zero, i.e., $\rho_{il,m} = 0$ for $l \neq m$. Moreover, since the PCS are considered to represent independent sources of variations, correlation between different parameters on different transistors is also taken to be zero., i.e., $\rho_{ij,kl} = 0$ for $i \neq k$ and $j \neq l$. This leaves only one set of non-zero entries in the correlation matrix between the same factor for different matched components, i.e., ρ_{iljl}.

Intra-die Principal Component Decomposition

The correlation matrix is further simplified by using a second level of PC decomposition, replacing a PC of the original model, e.g., f_j, by a linear combination of a set of second-level PCS representing the intra-die variation. The result of the second PC decomposition is a unified representation that captures both the correlation between the model parameters and the matched components. Moreover, the transformation maintains the correlation between the model parameters because the RV for each original PC is replaced by an equivalent equation with the same mean and variance. The second level PC transformation adds, at worst, n new PCS, resulting in a total of $n \times k$ PCS. Since the statistical SPICE model is independent of the application, the number of PCS k is fixed, and usually k « m, where m is the number of model parameters. This results in a mismatch simulation method that adds only $O(n)$ new RVs for a circuit with n matched components.

An advantage of the approach of the present invention is that in practice the number of factors required is scarcely the $n \times k$ factors required in the worst case. This happens for two reasons. First, not all k PCS required to capture the correlation of the model parameters are necessary for

representing mismatch. Usually, a much smaller number of variables are required. Second, because the amount of mismatch is typically very small, the correlation matrix is, in general, characterized by a small number of dominant eigenvalues. Therefore, using the equation that gives the fraction of total variance explained by the *k-th* PCS, the variance of the system can be well approximated by using a small number of PCS compared to the worst-case n.

For example, in the asymptotic case of perfectly matched devices, this method automatically produces only one PC (corresponding to the dominant eigenvalue) for each independent process factor, resulting in no increase in the number of RVs. In the intermediate situations between the worst-case and the asymptotic case, the approach of the present invention provides an approximation scheme where a small number of PCS can be selected to accurately approximate the correlation between the components.

Statistical SPICE Models with Mismatch

Mismatch characterization typically does not produce the correlation between PCS of a statistical SPICE model. Usually, the result of mismatch characterization is a set of coefficients for a mismatch model of device performance. For example, MOS transistor mismatch characterization often results in the coefficients of a Pelgrom-style model for threshold voltage (V_{Th}) and saturation current (I_{DSAT}) or the transistor gain-factor (k') (see the Pelgrom, et al reference cited above). To utilize this information in the representation described above it must be converted into correlation between PCS of the statistical SPICE model.

The procedure for determining the unified statistical representation starts with a statistical SPICE model for correlation between model parameters. A subset of the PCS of this model is selected for representing component mismatch. The selection is based on two considerations: the device characteristics for which mismatch has been characterized, and the weightings of the different PCS in the equation for each SPICE parameter that impact these device characteristics. For example, if mismatch characterization has been performed for threshold-voltage and gain-factor of longchannel MOSFETs, then PCS that have the most impact on the VTH0 and U0 (mobility) parameters of the BSIM3v3 model are selected. Once the PCS of the model without mismatch have been selected, a numerical optimization is performed to find the correlation between these factors in order to obtain the measured mismatch in device characteristics.

Each optimization results in the correlation of the selected PC for one set of device geometry and layout parameters. Repeating this procedure for different geometries and layout distances results in a set of correlation values that are either fit with an interpolating function or represented in a look-up table. This procedure results in a model of PC correlation as a function of device geometry and layout. The step of modeling PC correlation as a function of device geometry and layout is performed only once for a particular technology and layout style.

The method of the percent invention can be used as part of the Circuit Surfer statistical design and verification environment. This environment supports many tasks typically required for analog and mixed-signal design for manufacturability, such as statistical simulation, sensitivity analysis, response surface modeling, and circuit optimization for manufacturability. Mismatch

simulation is implemented in this environment as an annotation of the circuit netlist to specify the matched components, and annotations to the statistical SPICE models to include the effect of mismatch. The annotated netlist and SPICE models are used to derive a separate statistical SPICE model for each component using the two-level PCA. The modified netlist forms the input to Circuit Surfer. This implementation enables all the capabilities of statistical design for mismatch analyses such as variable screening, response surface modeling and Monte-Carlo using mismatch factors, and optimization of a design to reduce its mismatch sensitivity.

The use of the present invention is illustrated with two applications: a low voltage OPAMP and a D/A Converter. These topologies were implemented based on their continued significance in low voltage VLSI signal processing applications and their performances sensitivities to device mismatch characteristics.

Low Voltage OPAMP

The following is a description of an embodiment of the method, in accordance with the present invention, for statistical modeling and simulation of the impact of global variations and local mismatch on the performance of operational amplifiers (OPAMPs) of the type described. Such local mismatch and global variations are typically caused by random and systematic variations in the material composition, or in the processing steps that are used to fabricate the integrated circuits. Global variations affect integrated circuit devices by causing random differences in the electrical properties of the circuit elements, such as transistors, resistors, capacitors, memory cells, wires, etc., that are fabricated on different chips from the same wafer, on different wafers,

or on different batches of wafers. The local mismatch, or intra-die variations, are differences in the electrical properties of circuit elements that affect components of circuits that are fabricated on the same die. For example, two identically drawn transistors, fabricated next to each other in any particular chip, will still present different threshold voltage values.

The OPAMP is of the 2-stage rail-to-rail class-AB architecture shown in Figure 1 which employs a constant-g_m input stage with tail current control. The commonality of complimentary input stages in contemporary designs makes this topology ideal for exploring the effects of mismatch on offset voltage (*Vos*) given both NMOS and PMOS mismatch effects. In addition, low voltage design examples such as this help exploit the increasing dependence of proper signal resolution on low *Vos*. A Pelgrom model for the mismatch in the threshold voltage and gain factor of long-channel transistors is available for this class of technologies. For the matched NMOS pair M1-M2, the model specifies $\sigma(\Delta(Vth)) = 2mV$ and $\sigma(\Delta(k')) = 0.7$ %. For the PMOS pair M3-M4, the mismatch was: ($\sigma(\Delta(Vth)) = 1.5mV$ and $\sigma(\Delta(k')) = 0.45$ %, where *Vth* represents the MOSFET threshold voltage and *k'* represents the MOSFET gain factor.

A statistical SPICE model was estimated for the process technology used in this example. The model was estimated using measured variance and correlation between key transistor performances. This set of performances includes: transistor drive current in the linear and saturation regions (Idsat, Idlin) and transistor threshold voltage in the linear and the saturation region (Vtsat, Vtlin). The statistical SPICE model is represented in terms of principal factors, thus achieves the effect of first-level principal component decomposition.

The mismatch model described above is not suitable for direct use in circuit simulation. A SPICE level representation of mismatch is derived by selecting SPICE model parameters that effect long-channel threshold voltage and the gain factor. For BSIM3v3 SPICE models, these parameters are VTH0, TOX, and U0. Numerical optimization is performed to find the correlation between these factors in order to obtain the measured mismatch in threshold voltage and gain factor.

The statistical model including mismatch was used to simulate the impact of mismatch on key performance measures on this design. This simulation makes use of the method of this invention to perform the second level principle component decomposition. The impact of mismatch on this design is shown in Table 1.

Table 1: Impact of Mismatch on OPAMP (10,000 sample Monte-Carlo)

Performance	Without Mismatch		With Mismatch	
	Mean	std. dev	Mean	std. dev
Vos (mV)	-1.803	0.09627	-1.802	0.7216

A unified model is derived by applying the method described in the previous sections. The first level PCA results in nine first level PCS (pca1...pca7, pcaLint and pcaWint) for the four matched transistors, thus resulting in a 36 x 36 sparsified covariance matrix. A second level PCA is performed using this matrix. Three dominant eigenvalues explain over 98% of the total variance. In this way, it is possible to account for both inter-die and intra-die variations with the

addition of three variables. These three variables are suitably obtained by re-defining pca2, pca4 and pca5 as linear combinations of two independent components.

Two sets of Monte-Carlo simulations were performed, one using only the inter-die model and the second using the unified model. As expected, this design shows that *Vos* is extremely sensitive to mismatch. By quantifying the exact impact of mismatch the method of the present invention allows an accurate assessment of manufacturability of this topology. It also shows that parametric yield estimates can be overly optimistic for designs sensitive to mismatch if mismatch effects are not accounted for in statistical simulation or worst-case models. Figure 2 shows the distribution of *Vos* with and without mismatch. The overlay illustrates the 7X increase in the offset voltage standard deviation. Without the ability of efficient and accurate mismatch analysis the impact on parametric yield due to this increase would be missed.

D/A Converter

The D/A Converter shown in Figure 3 uses a binary weighted current implementation with eight-bit resolution. The output current is summed via current switching and output to a linear current/voltage (I-V) converter. Data converter non-linearity is a measure of the error induced by the converter and it is sensitive to the matching between the transistors comprising the ratioed current source.

Simulation with and without intra-die variation was carried out as described for the OPAMP. The procedure was deriving the statistical SPICE model using principal-factors and estimating a representation of device mismatch in form of a SPICE model are identical to those for the OPAMP. The simulation was carried out using the method of this invention. The mismatch effects were examined for the binary weighted current source identified in Fig. 3. Specifically, the analog output was tested for differential non-linearity (DNL), defined as the deviation of each set of adjacent steps at the analog output from their ideal value (1 LSB). Here, we have defined the performance specification to be +/- ½ LSB. The results of statistical simulation with and without intra-die effects are shown in Table 2.

Table 2: Impact of mismatch on D/A Converter (10,000 sample Monte-Carlo)

Performance	Without Mismatch		With Mismatch	
	Mean	std. dev	Mean	std. dev
DNL (LSB)	-0.176	0.086	-0.198	1.155
Yield	100%		34%	

Intra-die variation causes the standard deviation of DNL to increase by a factor of 13. Such a large increase in the increment causes large changes in the linearity of the D/A Converter. As in the previous example, including intra-die effects is vital to get accurate estimation of circuit performance variability, but since the circuit's performance for this topology depends upon the pairwise matching of eight different transistors, a complete statistical simulation using a standard methodology would entail running a Monte-Carlo experiment with large number of correlated RVs.

For example, a circuit with eight matched transistors and 7 to 12 independent sources of process variation (typical of advanced CMOS processes) requires the generation of a sequence of correlated random numbers for as many as 96 different RVs. Several thousand SPICE evaluations would be required to stabilize the Monte-Carlo results for such a high-dimensional system. The advantages of complexity reduction using second order principal component decomposition are illustrated by the graph depicted in Figure 4. This figure shows the standard deviation of DNL versus the number of additional factors employed for mismatch simulation. In fact, although in the worst case the present technique would require 18 additional RVs, by applying the screening methodology previously described under the heading "Intra-die Principal Component Decomposition" above, it is possible to model very accurately the impact of intra-die variability on the D/A Converter with only two additional variables. This result makes the simulation of mismatch applicable to an inherently larger set of matched transistors; a requirement as supply levels and feature sizes continually decrease and previously negligible device effects become increasingly significant.

CLAIMS

We claim:

1. A method for statistical modeling and simulation of the impact of global variation and local mismatch on the performance of integrated circuits, comprising the steps of:

   a) estimating a representation of component mismatch from device performance measurements in a form suitable for circuit simulation;

   b) reducing the complexity of statistical simulation by performing a first level principal component or principal factor decomposition of global variation, including screening;

   c) further reducing the complexity of statistical simulation by performing a second level principal component decomposition including screening for each factor retained in step b to represent local mismatch; and

   d) performing statistical simulation with the joint representation of global variation and local mismatch obtained in step c.

2. A method of modeling and simulating the impact of local mismatch on performance of integrated circuits comprising the steps of:

   a) estimating a representation of component mismatch in a form suitable for circuit simulation from device performance measurements;

   b) reducing the complexity of statistical simulation by performing principal component or principal factor decomposition for local mismatch, including screening; and

c) performing statistical simulation with local mismatch obtained in step b.

3. The method of claim 2 where the principal component or principal factor decomposition is performed using eigenvalue eigenvector decomposition.

4. The method of claim 1 where the first principal component or principal factor decomposition is performed using eigenvalue eigenvector decomposition.

5. The method of claim 1 where the second principal component or principal factor decomposition is performed using eigenvalue-eigenvector decomposition.

6. A method for statistical modeling and simulation of the impact of global variation and local mismatch on the performance of integrated circuits, wherein said method is integrated in a statistical design and optimization computer-aided design tool to perform statistical simulation of joint and separate impact of global variation and local mismatch on performance of integrated circuits and said method comprises the steps of:

a) estimating a representation of component mismatch from device performance measurements in a form suitable for circuit simulation;

b) reducing the complexity of statistical simulation by performing a first level principal component or principal factor decomposition of global variation, including screening;

c) further reducing the complexity of statistical simulation by performing a second level principal component decomposition including screening for each factor retained in step b to represent local mismatch; and

d) performing statistical simulation with the joint representation of global variation and local mismatch obtained in step c.

7. A method of modeling and simulating the impact of local mismatch on performance of integrated circuits, wherein said method is integrated in a statistical design and optimization computer-aided design tool to perform statistical simulation of joint and separate impact of global variation and local mismatch on performance of integrated circuits and said method comprises the steps:

a) estimating a representation of component mismatch in a form suitable for circuit simulation from device performance measurements;

b) reducing the complexity of statistical simulation by performing principal component or principal factor decomposition for local mismatch, including screening; and

c) performing statistical simulation with local mismatch obtained in step b.

8. The method of claim 7 where the principal component or principal factor decomposition is performed using eigenvalue eigenvector decomposition.

9. The method of claim 6 where the first principal component or principal factor decomposition is performed using eigenvalue eigenvector decomposition.

10. The method of claim 6 where the second principal component or principal factor decomposition is performed using eigenvalue-eigenvector decomposition.

ABSTRACT

A method of modeling and simulating the impact of global variation and local mismatch on the performance of integrated circuits includes the step of converting, if necessary, the device mismatch model at the device performance level into a model suitable for circuit simulation; for example, at the SPICE parameter level. Second, if global variation is provided, performing a first level principal-component or principal-factor decomposition and screening to represent the global variation. If no global variation is provided, this decomposition is performed for the local variation only. Third, performing a second level principal-component or principal-factor decomposition and screening for each independent factor identified in the second step to represent the local variation and reduce its dimensionality. If no global variation is provided in the initial model before local variation is applied, this step does not apply. Fourth, performing statistical circuit simulation and analysis with the combined set of independent factors that result from the second and/or third steps to estimate the impact of global and local variation jointly and/or separately on the circuit of interest.

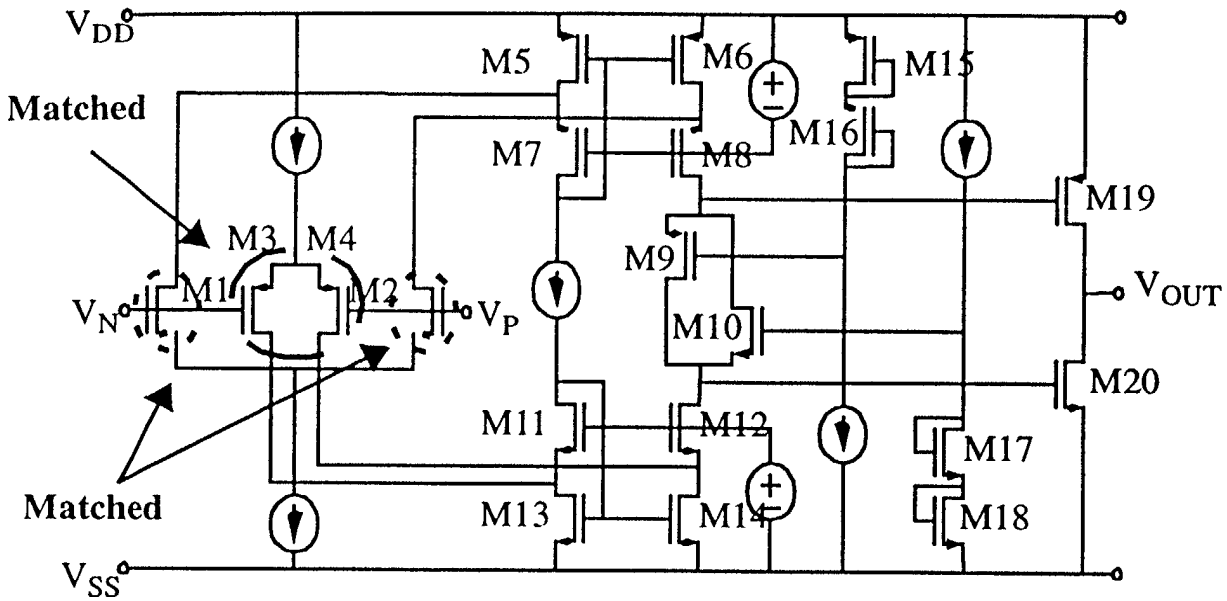
V_{DD}
Matched
M5
M6
M15
M16
M7
M8
M19
M3
M4
M9
M1
M2
V_N
V_P
V_{OUT}
M10
M20
M11
M12
M17
Matched
M13
M14
M18
V_{SS}

FIGURE 1

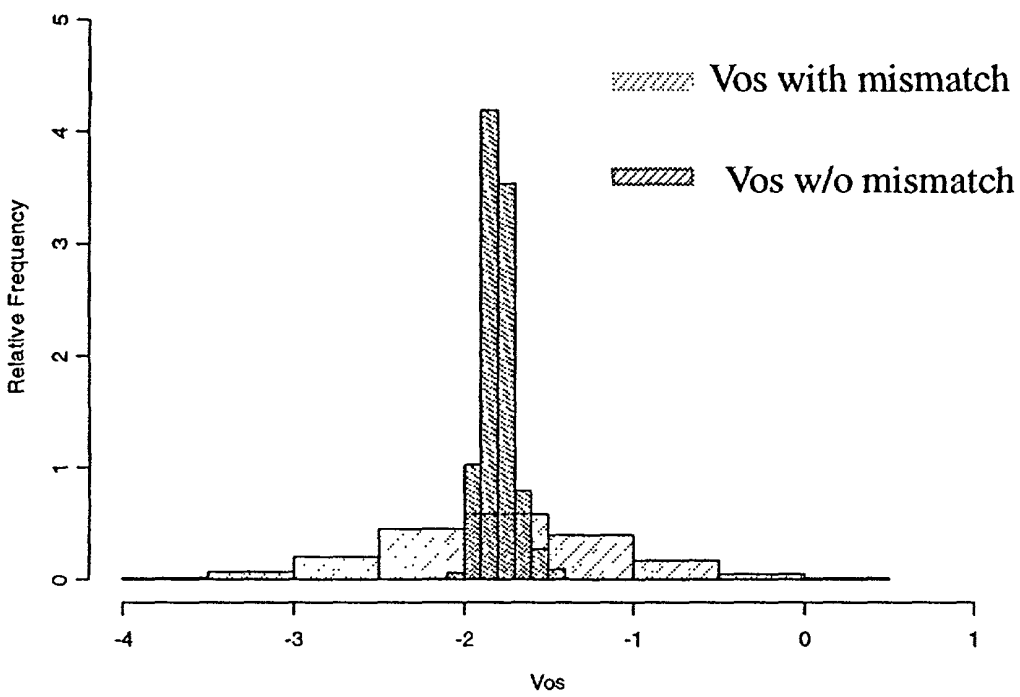

FIGURE 2

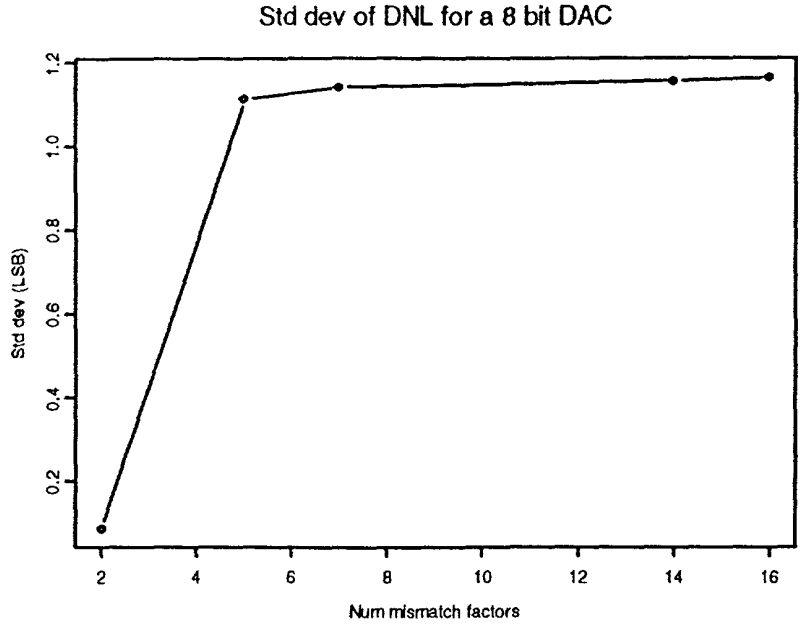

FIGURE 4

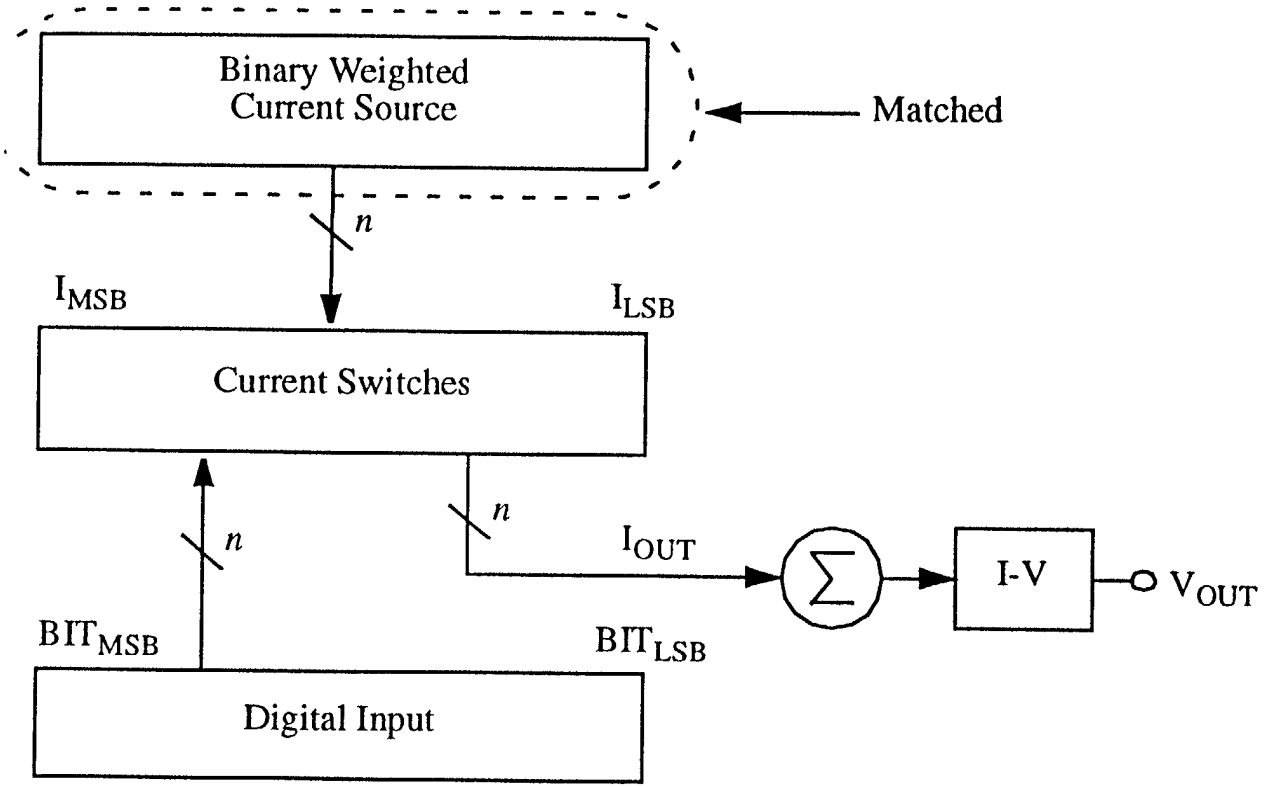
Binary Weighted
Current Source
Matched
n
I_{MSB}
I_{LSB}
Current Switches
n
n
I_{OUT}
Σ
I-V
V_{OUT}
BIT_{MSB}
BIT_{LSB}
Digital Input

FIGURE 3

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **EFFICIENT METHOD FOR MODELING AND SIMULATION OF THE IMPACT OF LOCAL AND GLOBAL VARIATION ON INTERGRATED CIRCUITS** the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

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I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Provisional Application No. 60/166,242 Filed 11/18/99

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under

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